Programme of **"Elettronica dei Sistemi Digitali 1"** ***" Digital Electronic Systems 1"***		
• CODE: **I0269.** • COMPULSORY. • 2ND CYCLE IN ELECTRONIC ENGINEERING, 1ST YEAR, 2ND SEMESTER.		
NUMBER OF ECTS CREDITS: 9 (LECTURE ACTIVITY IS AROUND 90 HOURS, WORKLOAD 225 HOURS; 1 CREDIT = 25 HOURS). COURSE STRUCTURE LECTURE: 7 HOUR PER WEEK.		
TEACHER: **MARCO FACCIO**		
1	**Course objectives**	The goal of this course is to focus on the Boolean logic fundamentals and its practical implications, needed to build the feasibility of modern digital electronic systems for both *ICT* and industrial applications. Particular attention is paid to methods and methodologies for modeling, description, formalization and development of significant key projects, as well as their practical achievements as a collection of finite state automata. On successful completion of this module, the student should have knowledge and understanding of fundamental concepts adopted for a modular top-down design of digital systems, using a set of finite state automata models. Besides the student should demonstrate capacity for defining and selecting appropriate strategies to solve the problems related to their physical implementation.
2	**Course content and Learning outcomes**	Topics of the module include: ***Introduction to digital system:*** Digital systems, Combinational and Sequential logic, Finite State Machine (FSM) and its models (Mealy and Moore), synchronous and asynchronous system, on real implementation of digital system (SSI and MSI circuits; PLD and FPGA systems – microprocessor systems). ***Combinational systems:*** boolean algebra, switches functions and gates, truth tables and combinational design, implicants and implicates, sum of product form or product of sum form, map and methods for minimizing boolean functions (Karnaugh maps, maps with entered variable, Quine -McCluskey algorithm), hazard strong design. MSI block: encoders, decoders, multiplexers, demultiplexers, comparators. Binary numbering systems and codes. Binary, octal and hexadecimal numbering systems. Codes. Negative numbers in sign and module, 1's complement, 2's complement. Application to binary arithmetic. ***Sequential systems:*** Flip-Flop function, Flip-Flop types: FF SR, FF SRE, FF JK, FF Master-Slave, FF edge triggered, FF T, FF D. Simple sequential systems: asynchronous counters; Synchronous sequencer, Register function and shift registers, PIPO, PISO, SIPO and SISO hardware core; set of register; Analysis of sequential networks. Timing diagrams. ***Finite state machine and its description:*** state-transition diagram, PS/NS table; Algorithmic State Machine flowchart (ASM) and its application to counters, sequencer and register control. ***Arithmetic hardware:*** Adders, half and Full Adder, ripple Adder, CLA, Carry skip adder, Subtractor, ALU; Multipliers: algorithm (sum loop), serial and parallel; Wallace multiplier, Booth's algorithm ***Register Transfer Model:*** Examples of analysis, design and synthesis of Control Units (based to FSM with ASM description) for Arithmetic block and "smart" register hardware. ***Introduction to programmable logic*** (HW + SW) Algorithmic approach to block HW design; from set of Moore machine to microprocessor architecture; selectable and programmable systems; VN architecture, Harvard architecture, ad hoc architectures. Outline of the architecture of microprocessors, microcontrollers, Digital Signal Processor (*DSPor*), Single Board Computer (*SBC*), Steps and tools for the development of a Logic Programmed design, Hw and SW integration.

		On successful completion of this module, the student should: - have profound knowledge of applied Boolean algebra, synthesis methods applied to both combinational and sequential systems (finite state automata); - be able to design a simple but significant project of a digital electronic system; - understand and explain the logic and electronic block scheme for a simple but meaningful digital system; - demonstrate skill in top-down modular partitioning of a digital system; - be able to read and understand other texts on related topics; - demonstrate capacity to communicate the results of technical works in a clear and coherent way, with the generation of systematic and meaningful documentation for any designed and assembled digital system.
3	**Prerequisites and learning activities**	The student must know: the fundamentals of algebra and Boolean algebra, the fundamentals of information representation and transcoding between different representations.
4	**Teaching methods and language**	Lectures and exercises. Language: Italian / English **Ref. Text books** **-** J. D. Daniels: *Digital Design from Zero to One* , J. Wiley. **-** M.M. Mano – C.K. Kime: *Logic and Computer Design Fundamentals* – Prentice Hall. - *Class notes written by the Lecturer* (in Italian).
5	**Assessment methods and criteria**	The exam will consist in a written test related to a simple digital project and in a discussion on any two topics from the course.