Programme of "Elettronica dei Sistemi Digitali 2"
" Digital Electronic Systems 2"

- CODE: I2I019.
- COMPULSORY.
- 2ND CYCLE IN ELECTRONIC ENGINEERING, 2ND YEAR, 1ST SEMESTER.

NUMBER OF ECTS CREDITS: 9 (LECTURE ACTIVITY IS AROUND 90 HOURS, WORKLOAD 225 HOURS; 1 CREDIT = 25 HOURS).
COURSE STRUCTURE LECTURE: 7 HOUR PER WEEK.

TEACHER: **MARCO FACCIO**

1	**Course objectives**	The primary aim of this course is completing the student's vision of all possible digital system implementations. This involves the study of issues related to achievements in Programmed Logic (microprocessor, microcontroller, Digital Signal Processor (*DSPor*) and so on) with reference to HW design. But the final and most important goal is providing ideas and tools to design complex digital systems using user-configurable VLSI circuits (FPGAs). Particular attention is paid to HW design of algorithms and to HW construction of SoC systems (with also *ad hoc* processing architectures). On successful completion of this course, the student should: understand the fundamental concepts of Programmed Logic; understand and manage issues related to HW development of projects based on microprocessors and/or DSPors, understand and manage the integration of "*application SW*" on designed HW, develop the capability to design configurable and programmable architectures for the direct algorithm implementation in HW.
2	**Course content and Learning outcomes**	Topics of the module include: ***THE FEASIBILITY OF DIGITAL SYSTEMS*** Technology feasibility aspects, logical and functional aspects of physical implementations; digital system as a collection of finite state automata, top-down and bottom-up approach; equivalence between in hardware directly implementation (hardwired logic) and GP Programmed Logic (*LP*)implementation (HW microprocessor + app.SW) realizations mixed with ad hoc programmable architectures; co-design methodologies. ***FROM THE HW-WIRED AUTOMATA TO LOGIC PROGRAM AUTOMATA IMPLEMETATION*** Step by step construction of a General Purpose (*GP*)programmable automaton; RTL synthesized as a set of modules to Moore; temporal base evolution; Multi-action systems; selection of a single action; arithmetic processing unit; control unit; control structures; GP architectures; construction of systems with ad hoc architectures; specific exercises for constructing HW "*programmable performer*" systems. ***CANONICAL ARCHITECTURES OF MICROPROCESSOR, MICROCONTROLLERS, DSPORS*** Fundamentals of algorithm control structures and their hardware implementation; VonNeuman (VN) microprocessor architecture, instruction set, addressing modes, the external world; internal- external communication interface, set of elementary actions; Example exercises for HW control unit design of the internal functions of VN microprocessor; architectures of microcontrollers (single chip); parallelization and execution time reduction of internal actions; impact on architectures, HW area and internal UC; Harvard architectures; architectures for DSPor, general principles, examples and comments on commercial DSPor architectures units, SBC with microprocessor, microcontroller, or DSPor; outline of the multiprocessor, multicore and multiprocessing architectures. ***WORKFLOW FOR THE REALIZATION OF PROGRAMMED LOGIC GP SYSTEMS*** (the development phases of a PL project, co-design methodologies) Design flow (HW development, appl. SW development, and its environments); simulation and emulation; module testing, integration between HW and SW, real-time constrains and guidelines to meet them; Logic Analyzer and In Circuit Emulator (ICE); summary of current technologies. ***BRIEF OVERVIEW ON THE SEMICONDUCTOR MEMORY ARCHITECTURES***

		Classification of semiconductor memories; internal architecture and operations of an SRAM; prevalently read-only memories; FG-MOS transistor; Internal structure of a flash memory. ***VLSI DIGITAL SYSTEMS CONFIGURED BY USER*** Historical evolution: EEPROM, PLD and FPGA; examples of FPGA circuit architectures; issues related to the implementation of user-defined architectures on the FPGA (eg, on Xilinx family); the problems of isomorphism; CAD development environment and tools (flow typical); - examples of project realization on FPGA. ***CAD ENVIRONMENT for the DESCRIPTION, SIMULATION and SYNTHESIS of COMPLEX DIGITAL SYSTEMS*** Introduction to VHDL: structures, syntax, reference circuits, examples and exercises at different levels of increasing complexity; automatic layout and simulation postlayout ; example of a complete environment for FPGA design (Xilinx, Altera). ***FPGA IMPLEMENTATION of uP and DSPor*** Xilinx MicroBlaze soft-core architecture system and flow configuration; Altera NIOS soft-core architecture system and flow configuration; brief on the implementation of soft-core processor in other manufacturers (ARM, Leon …); development, loading and execution of application SW on FPGA. ***BRIEF OVERVIEW ON ELECTRICAL PARAMETERS OF GATE AND ELECTRONIC SYSTEMS*** Electrical models of the logic gates; Logic gates with switching BJT and MOS transistors; working principle of TTL gates at various supply voltages; CMOS basic blocks; interfaces (TTL - CMOS) and (CMOS-TTL); CMOS gates in full custom; interface general problems with FPGA and/or ASIC; HW handling of I/O (communication with the outside) of the FPGA. ***FINAL EXAMPLE OF A PROJECT WITH A COMPLEX ARCHITECTURE SYSTEM.*** On successful completion of this course, the student should - have a profound knowledge of the methodologies and tools for the correct design of complex digital electronic systems; - have knowledge and understanding of issues related to the architectures for implementing digital systems by the programmed logic; - have knowledge and understanding of testing problems related to SW applications SW implemented on a HW system; - be able to read and understand data sheets of complex digital electronic components such as microprocessors or FPGAs; - have knowledge and understanding of basic concepts related to the realizations of digital electronic systems by means of user-configurable VLSI systems; - demonstrate skills at CAD tools, VHDL language and design of architectures for PL; - demonstrate capacity to read and understand other texts on related topics.
3	**Prerequisites and learning activities**	The student must have successfully completed the Digital Electronic Systems 1 course (or equivalent), and must also have a good knowledge of basic computer courses, C programming language and Matlab tools.
4	**Teaching methods and language**	Lectures, exercises and laboratory sessions with CAD tools. Language: Italian / English **Ref. Text books** - M.M. Mano – C.K. Kime: *Logic and Computer Design Fundamentals* – Prentice Hall - Lapsley P., Bier J., Shoham A., Lee E.A. - *DSP processor fundamentals* – IEEE Press - Wanhammar L. - *DSP Integrated Circuits* – AcademicPress - Technical Documents provided by companies Xilinx, Altera, Actel, Lattice ... - *Class notes written by the Lecturer* (in Italian)
5	**Assessment methods and criteria**	A lab project can be assigned to enforce the students to achieve the intended learning outcomes. As the exam is concerned, there is a free choice between two options: a) Written test related to a digital project and oral exam (3 questions); or b) development of laboratory project (using VHDL and FPGAs) and oral exam (2 questions).