UNIVERSITÀ DEGLI STUDI DELL'AQUILA
CORSI DI INGEGNERIA

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Curriculum scientifico

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Dati anagrafici e curriculari ? Giulio Giuseppe Marotta

Nome : Giulio Giuseppe MarottaLuogo e data di nascita : Rieti, 3 novembre 1952Residenza : Via Fontecerro Sud 18C - 02043 Contigliano (RI)Tel : 0746 - 707263Codice fiscale : MRT GGS 52S03H282RTitolo di studio: Laurea in Ingegneria Elettronica-La Sapienza - Roma Sede di lavoro: Micron Semiconductor Italia - Via A. Pacinotti 5/7 - Nucleo Industriale - 67051 Avezzano (AQ)Tel : 0863 - 456418 Esperienza professionale maturata :- Assunto da Texas Instruments Italia nel 1981 - 1 anno come Process e TestEngineer in impianto di assemblaggio di transistori discreti di potenza.- 18 anni come progettista di circuiti integrati e responsabile di progetto presso il dipartimento di Ricerca e Sviluppo della Texas Instruments Italia a Rieti, ad Avezzano (AQ) e presso il VLSI Design Center del Central Research Lab della Texas Instruments Incorporated ? Dallas- 15 anni, dal 1999, come Project Manager presso il Dipartimento di Ricerca e sviluppo della Micron Italia in Avezzano (AQ) Interessi di ricerca :circuiti analogici bipolari e CMOS, sistemi integrati mixed signal, convertitori A/D e D/A, interfacce contactless, reti neurali, memorie associative, pattern recognition, memorie non volatili a floating gate (EPROM, EEPROM, NOR-Flash, NAND-Flash) e RRAM, memorie ferroelettriche e spintroniche, metodologie di progetto e CADProgetti eseguiti:- SN94516 : circuito monolitico in tecnologia bipolare per il controllo di lampade di emergenza. - TCM 1715 : forchetta telefonica attiva in tecnologia bipolar- TCM 1725 : forchetta telefonica attiva in tecnologia bipolare - TCM 1745 : forchetta telefonica attiva in tecnologia bipolare- SN94512 : Car Check Controller monolitico in tecnologia bipolare- SN94914 : Circuito di interfaccia per sensore di livello d'olio termoresistivo. Tecnologia CMOS.- TCM 3642 : Transponder passivo integrato in tecnologia CMOS+Eeprom (primo al mondo con EEprom a bordo)- TMS 3637 : Trasmettitore / Ricevitore per controllo remoto. Tecnologia CMOS + Eeprom- TMS87C510 : 512Kbit EEprom con multiplexed I/O- TMS87C110 : 1 Mbit EEprom con multiplexed I/O- TLE2301 : Amplificatore Operazionale di potenza in tecnologia bipolare-jfet.- Libreria di moduli EPROM per applicazioni embedded in microcontrollori della famiglia TMS 370 C8/C16. - Libreria di moduli EEPROM per applicazioni embedded in microcontrollori della famiglia TMS 370 C8/C16 - Libreria di moduli FLASH EPROM per applicazioni embedded in micro controllori della famiglia TMS 370 C8/C16 e DSP della famiglia TMS 320. (prime flash embedded al mondo prodotte in volumi).

- Chips di memoria NOR-Flash per applicazioni wireless- Chips di memoria NAND-Flash multilivello fino a 4 bit per cella: http://www.micron.com/products/nand-flash/slc-nand http://www.micron.com/products/nand-flash/mlc-nand http://www.micron.com/products/nand-flash/tlc-nandAutore di 65 brevetti di invenzione industriale:

PAT. NO.	Title
8,407,400	Dynamic SLC/MLC blocks allocations for non-volatile memory
8,405,444	Voltage switching in a memory device
8,248,862	Source bias shift for multilevel memories
8,217,705	Voltage switching in a memory device
8,174,897	Programming in a memory device
8,144,525	Memory cell sensing using negative voltage
7,983,088	Programming in a memory device
7,978,556	On-chip temperature sensor
7,948,802	Sensing memory cells
7,701,776	Low power multiple bit sense amplifier
7,635,991	Output buffer strength trimming
7,630,265	On-chip temperature sensor
7,440,332	Low power multiple bit sense amplifier
7,403,423	Sensing scheme for low-voltage flash memory
7,324,381	Low power multiple bit sense amplifier
7,271,620	Variable impedance output buffer
7,238,981	Metal-poly integrated capacitor structure
RE39,697	Method of making floating-gate memory-cell array with digital logic transistors
7,206,240	Fast sensing scheme for floating-gate memory cells
7,200,041	Sensing scheme for low-voltage flash memory
7,161,376	Variable impedence output buffer
7,064,582	Output buffer strength trimming
7,057,416	Enhanced protection for input buffers of low-voltage flash memories
7,034,587	Conditioned and robust ultra-low power power-on reset sequencer for integrated circuits
7,034,575	Variable impedence output buffer
7,009,241	Metal-poly integrated capacitor structure
6,940,310	Enhanced protection for input buffers of low-voltage flash memories
6,924,676	Conditioned and robust ultra-low power power-on reset sequencer for integrated circuits
6,911,862	Ultra-low current band-gap reference
6,906,956	Band-gap voltage reference
6,898,131	Voltage and temperature compensated pulse generator
6,897,511	Metal-poly integrated capacitor structure
6,822,904	Fast sensing scheme for floating-gate memory cells
6,813,190	Methods of sensing a programmed state of a floating-gate memory cell

6,807,111	Voltage and temperature compensated pulse generator
6,801,079	Ultra-low current band-gap reference
6,795,343	Band-gap voltage reference
6,751,121	Flash memory array architecture
6,697,284	Flash memory array structure
6,697,283	Temperature and voltage compensated reference current generator
6,687,161	Sensing scheme for low-voltage flash memory
6,643,192	Voltage and temperature compensated pulse generator
6,628,142	Enhanced protection for input buffers of low-voltage flash memories
6,584,035	Supply noise reduction in memory device column selection
6,525,410	Integrated circuit wireless tagging
6,475,846	Method of making floating-gate memory-cell array with digital logic transistors
6,368,901	Integrated circuit wireless tagging
6,262,914	Flash memory segmentation
6,191,976	Flash memory margin mode enhancements
6,118,706	Flash memory block or sector clear operation
5,907,171	Method of making floating-gate memory-cell array with digital logic transistors
5,874,849	Low voltage, high current pump for flash memory
5,844,839	Programmable and convertible non-volatile memory array
5,815,026	High efficiency, high voltage, low current charge pump
5,732,021	Programmable and convertible non-volatile memory array
5,717,634	Programmable and convertible non-volatile memory array
5,715,195	Programmable memory verify "0" and verify "1" circuit and method
5,704,014	Voltage-current conversion circuit employing MOS transistor cells as synapses of neural network
5,703,807	EEPROM with enhanced reliability by selectable V.sub.PP for write and erase
5,563,959	Character recognition
5,557,569	Low voltage flash EEPROM C-cell using fowler-nordheim tunneling
5,457,771	Integrated circuit with non-volatile, variable resistor, for use in neuronic network
5,319,604	Circuitry and method for selectively switching negative voltages in CMOS integrated circuits
5,299,286	Data processing system for implementing architecture of neural network subject to learning process
5,274,743	Learning system for a neural net of a suitable architecture, physically insertable in the learning proc

Pubblicazioni :**A 3bit/cell 32Gb NAND flash memory at 34nm with 6MB/s program throughput and with dynamic 2b/cell blocks configuration mode for a program throughput increase up to 13MB/s** Marotta, G.G. ; Macerola, A. ; D'Alessandro, A. ; Torsi, A. ; Cerafogli, C. ; Lattaro, C. ; Musilli, C. ; Rivers, D. ; Sirizotti, E. ; Paolini, F. ; Imondi, G. ; Naso, G. ; Santin, G. ; Botticchio, L. ; De Santis, L. ; Pilolli, L. ; Gallese, M.L. ; Incarnati, M. ; Tiburzi, M. ; Conenna, P. ; Perugini, S. ; Moschiano, V. ; Di Francesco, W. ; Goldman, M. ; Haid, C. ; Di Cicco, D. ; Orlandi, D. ; Rori, F. ; Rossini, M. ; Vali, T. ; Ghodsi, R. ; Roohparvar, F.

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Publication Year: 2010 , Page(s): 444 - 445
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Engineering in Medicine and Biology Society, 1988. Proceedings of the Annual International Conference of the IEEE

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Instrumentation and Measurement Technology Conference, 1998. IMTC/98. Conference Proceedings. IEEE
Volume: 1
Digital Object Identifier: 10.1109/IMTC.1998.679839
Publication Year: 1998 , Page(s): 506 - 510 vol.1 IEEE Conference Publications | | Quick Abstract |PDF (408 KB) **A new low cost fingerprint recognition system on FPGA** Alilla, A. ; Faccio, M. ; Vali, T. ; Marotta, G. ; DeSantis, L.
Industrial Technology (ICIT), 2013 IEEE International Conference on
Digital Object Identifier: 10.1109/ICIT.2013.6505806
Publication Year: 2013 , Page(s): 988 - 993 IEEE Conference Publications | | Quick Abstract |PDF (883 KB) | HTML Full-Wave Modeling of Inductive Coupling Links forLow-Power 3D System IntegrationGiulio Antonini, Daniele Romano and Giovanni De Luca,Università degli Studi dell?Aquila, Aquila, Italy; TommasoVali, Giulio Marotta, and Luca De Santis, Micron Italia,Italy - 2013 IEEE International Symposium on Electromagnetic Compatibility - EMC 2013 - " Memory Card Resident Character Recognition System " Proceedings of the PC Card Symposium hosted by PCMCIA, May 92, Santa Clara (CA)- " A high speed embedded flash memory for DSP and MCU applications" Proceedings of the European Microprocessor and Microcontroller Seminar, 1996.- " Memoria Flash embedded per microcontrollori e DSP " Alta Frequenza, marzo-aprile 1997, p. 33- " Modulo di memoria E2PROM embedded single poly " Alta Frequenza, marzo-aprile 1997, p. 43- " Non volatile memory technologies with emphasis on Flash" IEEE Press Series on Microelectronic Systems John Wiley & Sons - Hoboken NJ - 2008